REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-9 are presently active; Claims 1-9 having been amended by way of the present amendment. No new matter was added.

In the outstanding Office Action, the specification was objected to. Claims 1-5 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koishikawa (U.S. Pat. No. 5,351,162) in view of Yang (U.S. Pat. No. 6,429,691).

Regarding the objection to the specification, it is respectfully submitted that the present amendments to the specification overcome the objection.

Regarding the 35 U.S.C. § 112, second paragraph, rejection, it is respectfully submitted that the present amendments to the claims overcome this rejection.

Regarding the asserted combination of Koishikawa and Yang, the Office Action relies on item 13 of Koishikawa "to control the on/off action of the power semiconductor switching elements." Yet, as presently clarified Claim 1 defines that a control unit synchronously repeats a regional control operation to operate a first group of the plural power semiconductor elements by providing a first input signal for each of the control electrodes of the first group, and thereafter to operate a second group of the plural power semiconductor elements by providing a second input signal for each of the control electrodes of the second group after an operation of the first group is finished. Pages 10 -12 of the specification describe the advantages of synchronized operation.

Koishikawa disclose the detection of fault conditions in respective plural MOSFET devices and the application of appropriate control signals in normal and fault conditions.

Yang dicloses the simultaneous switching of a pair of logic devices into opposite states.

Specifically, Yang in the section relied on by the Office Action discloses that:

> Transistor M5 is a pMOS, and transistor M6 is an nMOS. When an input voltage signal Vin is logic "HIGH" (in this case, VDD in CMOS logic level), ***the transistor M6 turns on and transistor M5 turns off.*** As the transistor M6 turns on, transistor M6 adds parallel resistance between node 1 and the ground (GND), so the resistance between transistor M6 and resistor R2 will be lower than resistor R4. Hence, the voltage at node 1 will go lower than that in node 2. For example, if resistors R1, R2, R3 and R4 are all, e.g., 1 kΩ, VDD and VCC are, e.g., 3 V, and the on-resistance of transistor M6 is designed to be, e.g., 1 kΩ, then the voltage at node 2 is, e.g., 1.5 V (3 V×1.0 kΩ/2.0 kΩ), and node 1 becomes, e.g., 1 V (3 V×.0.5 kΩ/1.5 kΩ). In this example, the PECL 100 input node 1 is 500 mV lower than the other input node 2, and in turn the base of transistor Q1 is lower than the base of transistor Q2. As a result, transistor ***Q1 turns off and transistor Q2 turns on*** allowing the tail current, It, flowing through the transistor Q2 to provide a voltage drop across load resistor RL2, e.g., (It)(RL2). Hence, the output Y becomes "HIGH" and Yb becomes "LOW" in PECL 100 level in FIG. 1. [emphasis added]

Thus, Yang discloses a gated logic circuit in which transistor M5 and transistor M6 (or Q1 and Q2) are automatically turned on and off at the same time.

There is no disclosure, suggestion, or motivation in Koishikawa or Yang to synchronously control the operation of one group of power semiconductor devices, and thereafter the operation of another group of power semiconductor devices, as defined in Claim 1.

Hence, Claim 1 and the claims dependent therefrom are believed to patentably define over Koishikawa and Yang.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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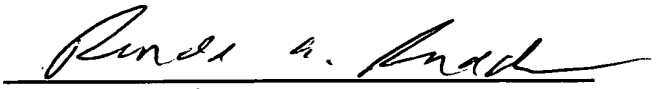

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